Course Code	TKEE163123
Course Name	Digital Systems Design
Course Instructors	Addin Suwastono; Risanuri Hidayat
Course Type	Selected Elective
Course Classification	Engineering Topics
Credit / Contact Hour per Week	3 / 150 minutes per Week
Course Description	The Digital Systems Design Course introduces the concepts and methods of designing simple sequential digital systems to complex sequential digital systems such as processor class. The Finite State Machine approach is applied in the design of simple sequential digital systems, while the algorithmic approach is applied in the design of complex digital sequential systems on the Register Transfer Level. Hardware description language (HDL) as a tool in the design of modern digital systems, will be introduced and used in this course.
Prerequisites Courses	Digital Technique
Covered Student Outcome	**Development of Engineering Solution (b)** **Engineering Design (c)**

Learning Outcome	1. Students are able to design a simple sequential digital system using the Finite State Machine (FSM) approach. (a) represents the behavior of a simple sequential system using state diagrams, ASM charts, and FSM state transition tables, and optimizing them. (b) design and analyze simple sequential digital systems. 2. Students are able to design complex digital sequential system with algorithmic approach at Register Transfer Level (RTL) level. (a) write computational algorithms using RTL notation. (b) map the computational algorithm to the datapath-controller structure. 3. Students are able to design and implement multiple digital circuits on FPGA, using Verilog HDL to describe the design.
Topic	1. Introduction 2. Approach Finite State Machine (FSM) 3. Algorithmic Approach 4. Introduction to Verilog HDL and Implementation on FPGA 5. Designing Microprocessors
Direct Asessment	

Direct Asessment Plan	**Measured Learning Outcome**
Assignments	LO1,LO2
Mid Exam	LO1,LO2
Final Exam	LO2,LO3

Indirect Assesment	Questionnaire (EDOM)
References	[1] Fundamentals of Digital Logic, with Verilog Design, Stephen Brown, Zvoko Vranesic,Mc Graw Hill 3rd Edition, 2014. [2] ***Digital Design with RTL Design, VHDL, and Verilog****, 2nd Edition by Frank Vahid, John Wiley and Sons, 2011.* [3] FPGA PROTOTYPING BY VERILOG EXAMPLES Xilinx SpartanTM-3Version, Pong P. Chu, John Wiley & Sons, Inc, 2008