Course Code	TKEE163123P
Course Name	Digital System Design Labwork
Course Instructors	Addin Suwastono, Agus Bejo, Sujoko Sumaryono, Risanuri Hidayat
Course Type	Selected Elective
Course Classification	Engineering Topics
Credit / Contact Hour per Week	1 / 150 minutes per Week
Course Description	This labwork provides a sequence of implementation exercise for digital system culminating in a microprocessor design. This labwork complements the topic discussed in the digital system design course by providing an implementation for each topics.
Prerequisites Courses	Digital System Design (TKEE163123)
Covered Student Outcome	**Engineering Design (c)** **Data and Experiment (d)** **Modern Tools Utilization (e)**

Learning Outcome	1. Students are able to understands the implementation of design approaches for digital system 2. Students are able to conduct experiment to demonstrate the design approaches for digital system 3. Students are able to operate Electronic FPGA Design Automation Tool to design digital systems
Topic	1. Introduction 2. Approach Finite State Machine (FSM) 3. Algorithmic Approach 4. Introduction to Verilog HDL and Implementation on FPGA 5. Designing Microprocessors
Direct Asessment	
Indirect Assesment	Questionnaire (EDOM)
References	[1] Fundamentals of Digital Logic, with Verilog Design, Stephen Brown, Zvoko Vranesic,Mc Graw Hill 3rd Edition, 2014. [2] ***Digital Design with RTL Design, VHDL, and Verilog****, 2nd Edition by Frank Vahid, John Wiley and Sons, 2011.* [3] FPGA PROTOTYPING BY VERILOG EXAMPLES Xilinx SpartanTM-3Version, Pong P. Chu, John Wiley & Sons, Inc, 2008

Direct Asessment Plan	**Measured Learning Outcome**
Lab Work Report	LO1 LO2 LO3
Pretest	LO1 LO2 LO3