

Course Code	TKIT161203
Course Name	Computer Architectures
Course Instructors	Risanuri Hidayat
Course Type	Required
Course Classification	Engineering Topics
Credit / Contact Hour per Week	2 / 100 minutes per Week
Course Description	The introduction and understanding of the architectural approaches applied to the design of modern computers, and their effect on the performance of computer system. Concepts used in computer architecture find application in other courses. In particular, the way in which the computer provides architectural support for programming languages and operating system facilities reinforces concepts from those areas.
Prerequisites Courses	Digital Technique
Covered Student Outcome	Fundamental Engineering Knowledge (a) Modern Tools Utilization (e) Engineering Awareness and Society (j)
Learning Outcome	<ol style="list-style-type: none"> 1. Students can explain the scope and materials to be given in the lecture. 2. Students can explain the parameters of computer system performance, calculate and evaluate the performance of computer systems based on various methods of performance measurement. 3. <ol style="list-style-type: none"> 1. Students can explain the function of the internal components of the processor and describe the structure of the interconnection between component. 2. Students understand the importance of instruction set, can explain the various operations, operands and addressing in the instruction set, can explain the advantages of RISC architecture. 3. Students can explain the concept of instruction pipeline in a processor, pipeline effect on processor performance improvement, weakness of pipeline architecture and how to overcome it. 4. <ol style="list-style-type: none"> 1. Students may explain the concept of hierarchical memory and their background. 2. Students can explain the various main memory and characteristics. 3. Students can explain the various structure and range of cache memory address mappings, explain the performance parameters of the cache memory and calculate the performance of the cache memory. 4. Students can explain the concept of virtual memories, virtual address translation - physical address, paging and segmentation differences, address translation effects, page / segment maps to virtual system memory performance. 5. Students can explain various external memories and performance calculations. 5. <ol style="list-style-type: none"> 1. Students can explain I / O components, interactions between I / O devices and CPU. 2. Students may explain the Operating System support in managing I / O activities. 6. <ol style="list-style-type: none"> 1. Students recognize and explain the various parallels in a single processor and the resulting performance improvements, distinguishing superscalar and VLIW architectures. 2. Students are able to recognize and explain various parallels to

	multiple processor systems, explaining the advantages and disadvantages of shared memory architecture and message passing architecture, explaining the parameters of multiprocessor system performance..												
Topic	<ol style="list-style-type: none"> 7. <i>Introduction</i> <ol style="list-style-type: none"> a. <i>Course description</i> b. <i>Components of a Computer System</i> c. <i>Development of Computer Architecture</i> 8. <i>Computer System Performance</i> <ol style="list-style-type: none"> a. <i>Performance Parameters</i> b. <i>Amdahl's Law</i> c. <i>Benchmarking</i> 9. <i>Central Processing Unit Architecture</i> <ol style="list-style-type: none"> a. <i>Processor Architecture</i> b. <i>Instruction Set</i> <ul style="list-style-type: none"> - <i>Instruction Set Architecture</i> - <i>Variety of Operations, Operand, and Addressing</i> - <i>RISC Architecture</i> c. <i>Instruction Pipeline</i> <ul style="list-style-type: none"> - <i>The Concept of Pipelining</i> - <i>Pipeline Hazards</i> 10. <i>Architecture memory</i> <ol style="list-style-type: none"> a. <i>The Hierarchical memory Concept</i> b. <i>Main memory</i> c. <i>Cache memory</i> d. <i>Virtual memory</i> e. <i>External memory</i> 11. <i>Input / Output Architecture</i> <ol style="list-style-type: none"> a. <i>I/O Interface</i> <ul style="list-style-type: none"> - <i>I/O devices</i> - <i>I/O Module</i> - <i>CPU Communication Technique</i> <ul style="list-style-type: none"> ● <i>Programmable I/O</i> ● <i>Interruption</i> ● <i>Direct Memory Access</i> b. <i>Operating System & I/O devices</i> 12. <i>Paralel Architecture</i> <ol style="list-style-type: none"> a. <i>Parallelism in Uniprocessor</i> <ul style="list-style-type: none"> - <i>Superscalar Architecture</i> - <i>VLIW Architecture</i> b. <i>Multiprocessor</i> <ul style="list-style-type: none"> - <i>Shared Memory Multiprocessor</i> - <i>Message Passing Multiprocessor</i> 												
Direct Assesment	<table border="1" style="width: 100%;"> <thead> <tr> <th style="width: 50%;">Direct Asessment Plan</th> <th style="width: 50%;">Measured Learning Outcome</th> </tr> </thead> <tbody> <tr> <td>Mid Exam</td> <td>LO1, LO2</td> </tr> <tr> <td>Final Exam</td> <td>LO3, LO4</td> </tr> <tr> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> </tr> </tbody> </table>	Direct Asessment Plan	Measured Learning Outcome	Mid Exam	LO1, LO2	Final Exam	LO3, LO4						
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Mid Exam	LO1, LO2												
Final Exam	LO3, LO4												
Indirect Assesment	Questionnaire and direct communication												
References	[1] William Stallings, Computer Organization And Architecture, Designing For Performance, 8th Edition, Pearson Education, Inc., 2010												

	[2] Hennessy, John L. and David A. Patterson, Computer Architecture: a Quantitative Approach (4th edition), Morgan Kaufmann, 4th edition, 2006.
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